What Is Claimed Is:

1. A semiconductor device having a main processor and a coprocessor for data processing, comprising:

a main program memory for storing main processor instructions and a first portion of coprocessor instructions;

a coprocessor program memory for storing a second portion of coprocessor instructions; and

a predecoder for predecoding at least one bit of each instruction fetched from the main program memory and for generating an active coprocessor control signal upon predecoding a coprocessor type instruction, wherein the second portion of coprocessor instructions are fetched directly from the coprocessor program memory and said first portion and said second portion of coprocessor instructions are processed by the coprocessor upon receipt of the active coprocessor control signal.

2. The device of claim 1, wherein said coprocessor active control signal and said main processor are synchronized to a system clock.

3. The device of claim 1, wherein the main processor instructions are m-bits and the coprocessor instructions are m+n bits, the n-bits being stored in the coprocessor program memory.

4. The device of claim 3, wherein said m-bits of said main processor instruction are fetched from the main program memory by the main processor and sent to the coprocessor after buffering by an instruction fetch buffer of said main processor.

5. The device of claim 4, wherein said m-bits are further sent through an instruction register in said main processor before being forwarded to the coprocessor.

6. The device of claim 3, wherein said m bits are forwarded directly to the coprocessor from the main program memory and the n bits are forwarded directly to the coprocessor from the coprocessor program memory.

7. The device of claim 3, wherein said m bits and n bits are forwarded to an instruction register in the coprocessor for latching in response to said active coprocessor control signal.

8. The device of claim 7, wherein said m bits and n bits are forwarded to a buffer prior to the register in the coprocessor for buffering.

9. The device of claim 1, wherein each of the main processor instructions and each of the coprocessor instructions are fetched from a common program address generated by the main processor.

10. A method of data processing in a semiconductor device having a main processor and a coprocessor, said main processor for executing m bit instructions, said coprocessor for executing m+n bit coprocessor instructions, the method comprising the steps of:

fetching by the main processor an m-bit instruction from a main program memory addressed by a program address; and

fetching by the coprocessor an n-bit instruction from a coprocessor program memory addressed by the program address upon decoding a predefined coprocessor code by the main processor.

11. The method of claim 10, wherein said step of decoding a coprocessor code is performed by a predecoder of the main processor, the predecoder for decoding c-bits of said m-bits,

said c-bits being predesignated to signify a coprocessor operation.

12. The method of claim 11, wherein said c-bits is at least one bit.

13. The method of claim 11, further including the step of forwarding said instruction fetched from the main memory to said coprocessor to form a coprocessor instruction of (m-c)+n bits.

14. The method of claim 10, wherein said fetching steps by the main processor and the coprocessor are synchronized to a system clock.

15. The method of claim 14, wherein said fetching steps by the main processor and coprocessor occur within a system clock cycle.

16. The method of claim 10, further including the steps of generating an active coprocessor control signal upon decoding by a predecoder the predefined coprocessor code and synchronizing said active coprocessor control signal to a system clock to form a control clock CCLK.

17. The method of claim 16, further including the step of latching the MSB portion of a coprocessor instruction sent from the main processor memory and the LSB portion of the coprocessor instruction from the coprocessor program memory in response to the control clock CCLK.